AMENDMENTS TO THE CLAIMS

This listing of claims will replace all prior versions and listing of claims in the application.

1. (Previously Presented) A method of forming at least one dielectrically insulating isolation trench for dielectric isolation of regions of different potential of device structures formed above an SOI wafer including an active semiconductor layer, by forming at least one void in said at least one isolation trench, thereafter forming a hermetically tight seal of the at least one void with respect to the semiconductor wafer surface, the method comprising:

performing a first fill in the form of a controlled deposition adapted to trench geometry with an aspect ratio of 15 to 1 or higher to thereby form oxide layers at trench walls, said oxide layers having an increasing thickness towards upper trench edges and forming a first bottleneck;

subsequently anisotropically RIE etching the oxide layers in a first step until the oxide layers are removed from the wafer surface and subsequently continuing the RIE etching process in a second step for removing the oxide layers in an upper trench portion to a defined depth for defining a later sealing portion of the at least one void by displacing downwardly the first bottleneck to form a further bottleneck.

2. (Cancelled)

3. (Previously Presented) The method according to claim 1, further comprising a second oxide deposition performed by a low pressure CVD process, thereby again depositing an oxide near a step formed by the further bottleneck to seal the at least one void located therebelow, said second oxide deposition being stopped when the portion of the oxide layer above said at least one void is grown above a wafer level of the semiconductor layer.

4. (Previously presented) The method according to claim 3, wherein after sealing said trench, the wafer surface is planarized and a technological process sequence is continued.

5. (Previously Presented) The method according to claim 1, wherein the RIE etching of the first trench filling in the area outside said trench stops on a polysilicon layer, which has previously been formed on at least one of a silicon dioxide layer and a multi insulator layer.

6. (Previously presented) The method according to claim 3, wherein the same process technique is used during the first and the second depositions.

7. (Previously presented) The method according to claim 3, wherein different process techniques are used during the first and the second depositions.

8. (Previously presented) The method according to claim 1, wherein said SOI wafer comprises micro electronic mechanic systems (MEMS) in a semiconductor layer formed on the oxide layer.

9. (Cancelled).

10. (Previously presented) The method according to claim 3, wherein the formed sealed of the at least one void is located below the level of the surface of the active semiconductor layer.

11. (Previously presented) The method according to claim 1, wherein a surface of the sealed trench is planarized.

12. (Cancelled)

13-19. (Cancelled)